## REMARKS

This paper is responsive to an Office Action dated November 29, 2005. Prior to this response, claims 16-17 and 20-28 were pending. After amending claim 16, claims 16-17 and 20-28 remain pending.

In Section 4 of the Office Action claims 16-17, 21-22, and 25-26 have been rejected under 35 U.S.C. 103(a) as unpatentable with respect to Halliyal (US 6,451,641), in view of Tiwari (US 2004/0108537). With respect to claim 16, the Office Action acknowledges that Halliyal does not describe the steps of forming a gate stack, where a dielectric material is exposed to an ionized species, to create charge trapping centers. The Office Action also states that Tiwari suggests exposing Halliyal's dielectric to an ionized species, with the advantages of a thinner gate dielectric, long retention times, reasonable low power, and high endurance. This rejection is traversed as follows.

An invention is unpatentable if the differences between it and the prior art would have been obvious at the time of the invention. As stated in MPEP § 2143, there are three requirements to establish a *prima facie* case of obviousness.

> First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaeck* 947 F.2d 488, 20 USPQ2d, 1438 (Fed. Cir. 1991).

As noted in the Applicant's specification, one purpose of the claimed invention is to replace the conventional oxide-nitride-oxide (ONO) gate multilayer stack, as used in a NROM or MONOS memory device, with a single layer of high-k dielectric that has been plasma treated to enhance its charge trapping characteristics (page 2, ln. 23 through page 3, ln. 25). In the ***Response to Arguments*** Section the Office Action correctly states that NROM and MONOS devices are not recited in the claimed invention. These features are described, however, in the prior art references (primarily the Background of the claimed invention and the Background of Tiwari). An understanding of prior art is helpful in discussion the issue of motivation. As presented in more detail below, Tiwari's solution to the problems associated with MONOS devices points away from the claimed invention solution to the same problem.

Halliyal generally describes a MOS transistor made with a high-k dielectric (Abstract). The novelty of Halliyal's invention appears to be a method of forming a polySi gate electrode that does not "reduce" the underlying high-k dielectric gate insulator (col. 5, ln. 27-46). Halliyal mentions that his device may be used as a FET in an EEPROM memory. However, Halliyal does not describe either a NROM or MONOS memory device, or any kind of transistor that operates on a charge trapping or floating gate principle. More particularly, Halliyal does not describe the steps of exposing a high-k dielectric material to an ionized species, inducing charge trapping centers in the high-k dielectric material as a result of the exposure, or a device where charge can be trapped in a gate stack.

Tiwari describes a memory device that includes a charge trapping region 20 (Fig. 1). The charge trapping region 20 includes an

injection layer 50 of silicon dioxide, a charge trapping layer 52 of silicon nitride, and a control layer 54 of silicon dioxide (Fig. 2, [0037]). The oxide/silicon nitride/oxide (ONO) charge trapping region 20 is separated from the transistor gate, source, and drain by an intervening semiconductor layer 24. Some additional charge trapping region materials are mentioned in [0045], but it is not clear which particular layer(s) of the charge trapping region is being discussed in this paragraph. Figs. 14a through 15d depict an oxide/silicon nitride/oxide (ONO) charge trapping region.

In [0004] Tiwari describes a conventional ONO memory transistor. Tiwari states that the presence of a charge trapping layer located between the channel and gate has proven impractical as the dimensions of devices continues to scale smaller. Tiwari's solution to the problem is to retain the convention ONO charge trapping structure, where the charge trapping layer is buffered by top and bottom oxide layers, but to move the charge trapping layer from the gate, to under the channel backside. "A feature of the structure is in placing the storage of carriers on the back side of the transistor channel. This allows one to obey the insulator thickness constraints required for long-term storage in a memory while letting the gate oxide of the transistor be scaled for good operation of the device" [0040].

The clarify the description of the invention, claim 16 has been amended to specifically recite that the high-k dielectric is formed between the gate electrode and the channel, without intervening oxide layers. That is, the gate dielectric (with the charge trapping centers) is formed without an underlying oxide layer, and without an overlying oxide layer.

With respect to the first *prima facie* requirement, there must be some suggestion in the Tiwari reference to modify Halliyal in a manner that makes the claimed invention obvious. Here, the combination of references clearly points away from the claimed invention. Halliyal does not describe a transistor gate dielectric with charge trapping centers. Tiwari suggests that the charge trapping region must be formed using an ONO-like structure, where an oxide insulator is formed on either side of the actual charge trapping layer. Further, Tiwari suggests that the charge trapping region must be moved from the transistor gate, to the channel backside, to minimize interference with gate dielectric thickness.

Considered from the perspective of the second *prima facie* requirement, even if an expert were given the Halliyal and Tiwari inventions as a foundation, there is no reasonable expectation that this expert could derive the claimed invention, since neither reference acknowledges that a charge trapping region can be (optimally) formed in a gate stack. Further, neither reference suggests that a charge trapping region can be formed from a single layer of dielectric.

With respect to the third *prima facie* requirement, even if the references are combined, they do not disclose all the elements of the claimed invention. Applicant's claim 16 recites the steps of forming a gate stack with a single layer of a charge trapping high-k dielectric, without underlying/overlying oxide insulator layers. As noted above, Halliyal does not address the subject of charge trapping. Tiwari only describes a charge trapping region formed in an ONO-like structure with top and bottom oxide insulators. Further, Tiwari states that the ONO charge trapping region should not be formed in a gate stack. The combination of references does not explicitly describe all the steps of claim 16. Neither

does the combination of references suggest any modifications that make these limitations obvious. Claims 17, 21-22, and 25-26, dependent from claim 16, enjoys the same distinctions from the cited prior art, and the Applicant requests that the rejection be removed.

In Section 12 of the Office Action, claim 20 has been rejected under 35 U.S.C. 103(a) as unpatentable with respect to Halliyal and Tiwari, in view of Afanas'ev (2001/0015453). The Office Action acknowledges that Halliyal and Tiwari do not describe oxygen, nitrogen, and hydrogen plasmas. The Office Actions states that "Afanas'ev teaches that nitrogen increases trapping centers in Halliyal's trapping layer and, therefore can be used to diminish the degrading impact of hole trapping". This rejection is traversed as follows.

In his Conclusions, Afanas'ev states that nitrogen impurities can be used to enhance electron trapping in Al2O3, ZrO2, and HfO2 materials. However, Afanas'ev never describes any type of implantation process. More specifically, Afanas'ev only describes as-deposited nitrogen-containing films (Abstract). Since Afanas'ev does not discuss the subject of ion implantation, it is difficult to image how Afanas'ev can suggest any modifications to Tiwari's ion implantation. In the ***Response to Arguments*** Section, the Office Action states that, "(t)here is no teaching in Afanas'ev against the incorporation of nitrogen using the ion implantation of Tiwari." However, the Applicant respectfully submits that a *prima facie* case for obviousness cannot be established based upon the subject matter *not* taught by a reference.

With respect to the third *prima facie* requirement, even if the references are combined, they do not disclose all the elements of the claimed invention. Applicant's claim 16 recites forming a gate stack with

a single layer of a charge trapping high-k dielectric, without underlying/overlying oxide insulator layers. None of the references explicitly describes these steps. Neither does the combination of references suggest any modifications that make these limitations obvious. Claim 20, dependent from claim 16, enjoys the same distinctions from the cited prior art, and the Applicant requests that the rejection be removed.

In Section 14 of the Office Action claim 23 has been rejected under 35 U.S.C. 103(a) as unpatentable with respect to Halliyal and Tiwari, and further in view of Chooi (US 6,486,080) and Agarwal (US 2001/0015453). The Office Action acknowledges that Halliyal does not describe a densification annealing, but that Chooi and Agarwal do. The Office Action states that it would have been obvious to follow the deposition of Halliyal's trapping layer with an annealing to cure oxygen vacancies. This rejection is traversed as follows.

At col. 6, ln 5-7, Chooi describes the densification of a metal oxide. At paragraph [0005] Agarwal describes densification to cure oxygen vacancies in a high-k dielectric. It is not clear how these references have any application to the claimed invention, which performs a densification annealing to prevent delamination of the gate (specification, page 12, ln. 24-25). Further, neither of these references describes ion implantation processes, the use of a high-k dielectric as a charge trapping material, or the use of a high-k dielectric memory device. Rather, it appears as if the various references have been assembled as the result of a retrospective search, using the limitations of claim 23 as keywords. These references do not suggest any modifications to Tiwari's ion implantation. Likewise, these references do not suggest modifications to Halliyal's high-k dielectric reduction protection process.

With respect to the third *prima facie* requirement, even if the references are combined, they do not disclose all the elements of the claimed invention. Applicant's claim 16 recites forming a gate stack with a single layer of a charge trapping high-k dielectric, without underlying/overlying oxide insulator layers. None of the references explicitly describes these steps. Neither does the combination of references suggest any modifications that make these limitations obvious. Claim 23, dependent from claim 16, enjoys the same distinctions from the cited prior art, and the Applicant requests that the rejection be removed.

In Section 16 of the Office Action claim 24 has been rejected under 35 U.S.C. 103(a) as unpatentable with respect to Halliyal and Tiwari, and further in view of Liang (US 5,372,957). The Office Action acknowledges that Halliyal does not describe a drain/source angle implant, as described by Liang. The Office Action states that it would have been obvious to form Halliyal's source/drain regions using Liang's process, to protect the transistor from hot carrier degradation. This rejection is traversed as follows.

Even if Liang does describe an angle implant to form source/drain regions, it is not apparent that Liang suggests any modifications to a process that ion implants an ONO-like charge trapping region (Tiwari), or to Halliyal's high-k dielectric reduction protection process. Therefore, with respect to the third *prima facie* requirement, the combination of references does not disclose all the elements of the claimed invention. Applicant's claim 16 recites forming a gate stack with a single layer of a charge trapping high-k dielectric, without underlying/overlying oxide insulator layers. None of the references explicitly describes these steps. Neither does the combination of references suggest any

modifications that make these limitations obvious. Claim 24, dependent from claim 16, enjoys the same distinctions from the cited prior art, and the Applicant requests that the rejection be removed.

In Section 18 of the Office Action claim 27 has been rejected under 35 U.S.C. 103(a) as unpatentable with respect to Halliyal and Tiwari, and further in view of Forbes (US 6,140,181). The Office Action acknowledges that Halliyal and Tiwari do not describe an ion energy or dosages, as described by Forbes.

However, even if the above-mentioned references can be combined, they do not disclose all the elements of the claimed invention. With respect to the third *prima facie* requirement, Applicant's claim 16 recites forming a gate stack with a single layer of a charge trapping high-k dielectric, without underlying/overlying oxide insulator layers. None of the references explicitly describes these steps. Neither does the combination of references suggest any modifications that make these limitations obvious. Claim 27, dependent from claim 16, enjoys the same distinctions from the cited prior art, and the Applicant requests that the rejection be removed.

In Section 19 of the Office Action claim 28 has been rejected under 35 U.S.C. 103(a) as unpatentable with respect to Halliyal and Tiwari, and further in view of Mosiehi (US 5,846,883). The Office Action acknowledges that Halliyal and Tiwari do not describe an ICP plasma source, as described by Mosiehi.

However, even if the above-mentioned references can be combined, they do not disclose all the elements of the claimed invention. With respect to the third *prima facie* requirement, Applicant's claim 16 recites forming a gate stack with a single layer of a charge trapping high-

k dielectric, without underlying/overlying oxide insulator layers. None of the references explicitly describes these steps. Neither does the combination of references suggest any modifications that make these limitations obvious. Claim 28, dependent from claim 16, enjoys the same distinctions from the cited prior art, and the Applicant requests that the rejection be removed.

It is believed that the application is in condition for allowance and reconsideration is earnestly solicited.

Respectfully submitted,

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